REMARKS

Claim 1 is currently active.

Two terminal disclaimers to obviate a double patenting rejection are included with this response, per the Examiner's request.

The Examiner has rejected Claim 1 as being anticipated by applicants' admitted prior art. Applicants respectfully traverse this rejection. It is respectfully submitted all that applicants stated was that DRAM chips do exist. Furthermore, applicants indicated to accomplish the transfer of an entire cell at a time many DRAM chips had to be used. That is all the stated in the background of the invention. Claim 1 also has the limitation of "a mechanism for reading or writing the entire ATM cell from or into the memory in one memory cycle". There is no teaching or suggestion of a mechanism for reading or writing the entire ATM cell from or into the memory in one memory cycle described in the background. Simply because applicants have suggested that the plurality of DRAM chips will be needed to read the entire ATM cell at a time does not also admit or indicate how such a mechanism would be accomplished to actually store the ATM cell in one memory cycle. Accordingly, Claim 1 cannot be anticipated by applicants' admitted prior art because this element is missing from the admitted prior art.

In view of the foregoing amendments and remarks, it is respectfully requested that the outstanding rejections and objections to this application be reconsidered and withdrawn, and Claim 1, now in this application be allowed.

Respectfully submitted,

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I hereby certify that this correspondence is being deposited with the U.S. Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on 8/19/05

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